

What is claimed is:

1. A contact comprising:  
a polysilicon layer formed on a substrate;  
one or more barrier layers formed above the polysilicon layer; and  
a barrier structure encircling the polysilicon layer and the one or more barrier layers.
2. The contact of claim 1, wherein the one or more barrier layers formed above the polysilicon layer is two.
3. The contact of claim 1, wherein the barrier structure is fabricated from tungsten nitride.
4. A contact comprising:  
a polysilicon layer formed on a substrate;  
a silicon barrier layer formed above the polysilicon layer;  
an oxygen barrier layer formed above the silicon barrier layer; and  
a barrier structure encircling the polysilicon layer, the silicon barrier layer, and the oxygen barrier layer.
5. The contact of claim 4, wherein the silicon barrier layer has a thickness of between about 900 and 1100 angstroms.
6. The contact of claim 4, wherein the oxygen barrier layer is fabricated from platinum-iridium.
7. A contact comprising:  
a polysilicon layer formed above a substrate;  
one or more barrier layers formed above the polysilicon layer; and

a silicon nitride barrier structure encircling the polysilicon layer and the one or more barrier layers.

8. The contact of claim 7, wherein at least one of the one or more barrier layers is fabricated from platinum-rhodium.

9. The contact of claim 7, wherein the polysilicon layer has a thickness of between about 450 angstroms and 550 angstroms.

10. A contact comprising:

a polysilicon layer formed on a substrate;

one or more barrier layers formed above the polysilicon layer; and

a barrier structure including an air gap and an oxide encircling the one or more barrier layers.

11. The contact of claim 10, wherein at least one of the one or more barrier layers is ruthenium silicide.

12. The contact of claim 10, wherein the barrier structure is an oxide layer.

13. A contact comprising:

a polysilicon layer formed on a substrate;

a silicon barrier layer formed above the polysilicon layer;

an oxygen barrier layer formed above the silicon barrier layer; and

a barrier structure encircling the silicon barrier layer and the oxygen barrier layer.

14. The contact of claim 13, wherein the silicon barrier layer is tungsten nitride.

15. The contact of claim 13, wherein the oxygen barrier layer is encircled by an air gap.

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16. A contact comprising:  
a polysilicon layer formed on a substrate;  
a tungsten nitride layer formed above the polysilicon layer;  
a ruthenium silicide layer formed above the tungsten nitride layer; and  
a barrier structure encircling the tungsten nitride layer and the ruthenium silicide layer.
17. The contact of claim 16, wherein the tungsten nitride layer has a thickness of between about 900 angstroms and 1100 angstroms.
18. The contact of claim 16, wherein the polysilicon layer has a thickness of about 500 angstroms.
19. An integrated circuit comprising:  
a first device;  
a second device;  
a contact coupling the first device to the second device; and  
an barrier structure encircling the contact.
20. The integrated circuit of claim 19, wherein the first device is a capacitor.
21. The integrated circuit of claim 19, wherein the second device is a transistor.
22. An integrated circuit comprising:  
a first device;  
a second device;  
one or more layers coupling the first device to the second device, at least one of the one or more layers is capable of blocking oxygen atom migration; and  
an structure encircling the one or more layers.

*mult 26* 23. The integrated circuit of claim 22, wherein the first device is a capacitor.

24. The integrated circuit device of claim 22, wherein the second device is a MOSFET.

*mult 27* 25. An integrated circuit comprising:

a first device;

a second device;

one or more layers coupling the first device to the second device, at least one of the one or more layers is capable of blocking silicon atom diffusion; and

a structure encircling at least two of the one or more layers.

26. The integrated circuit of claim 25, wherein the one or more layers is three.

*mult 28* 27. The integrated circuit of claim 25, wherein the structure is fabricated from an oxide.

*mult 29* 28. An integrated circuit comprising:

a first device;

a second device;

a multilayer contact including ruthenium silicide, the multilayer contact coupling the first device to the second device; and

an oxide ring encircling the ruthenium silicide.

29. The integrated circuit of claim 28, wherein the multilayer contact includes a polysilicon layer.

*mult 30* 30. The integrated circuit of claim 29, wherein the polysilicon layer is separated from the oxide ring by an air gap.

- mult 11*
31. An integrated circuit comprising:  
a first device;  
a second device;  
one or more layers coupling the first device to the second device, at least one of  
the one or more layers is capable of blocking oxygen atom migration; and  
an oxide ring structure encircling at least two of the one or more layers.
- mult 12*
32. The integrated circuit of claim 31, wherein at least one of the one or more layers  
is fabricated from a tungsten nitride.
- mult 13*
33. The integrated circuit of claim 32, wherein the oxide ring structure is in contact  
with the tungsten nitride.
- mult 14*
34. An integrated circuit comprising:  
a first device;  
a second device;  
one or more layers electrically coupling the first device to the second device, at  
least one of the one or more layers is capable of blocking the diffusion of silicon; and  
an oxide ring structure encircling at least one of the one or more layers.
- mult 15*
35. The integrated circuit of claim 34, wherein at least one of the one or more layers  
is ruthenium silicide.
36. The integrated circuit of claim 34, wherein the second device is an active device.
37. A memory cell comprising:  
a capacitor;  
a transistor;  
a contact structure coupling the capacitor to the transistor; and  
an insulating structure encircling the contact structure.

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38. The memory cell of claim 37, wherein the transistor is a metal-oxide semiconductor field-effect transistor.
  39. The memory cell of claim 37, wherein the contact includes one or more layers.
  40. A memory cell comprising:
    - a capacitor;
    - a metal-oxide semiconductor field effect transistor (MOSFET);
    - a contact structure coupling the capacitor to the MOSFET; and
    - an insulating structure encircling the contact structure.
  41. The memory cell of claim 40, wherein the MOSFET has a source and the contact couples the capacitor to the source.
  42. The memory cell of claim 41, wherein the contact includes at least two barrier layers.
  43. A memory cell comprising:
    - a capacitor;
    - a metal-oxide semiconductor field-effect transistor (MOSFET);
    - a contact structure including a polysilicon layer, a tungsten nitride layer, and a platinum-iridium layer, the contact coupling the capacitor to the MOSFET; and
    - an insulating structure encircling the contact structure.
  44. The memory cell of claim 43, wherein the insulating structure is fabricated from a tungsten nitride.
  45. The memory cell of claim 43, wherein the contact structure separates the platinum-iridium layer from the polysilicon layer.

46. A memory cell comprising:
  - a capacitor;
  - a metal-oxide semiconductor field effect transistor (MOSFET);
  - a contact structure including a polysilicon layer, a tungsten nitride layer, and a platinum-ruthenium layer, the contact coupling the capacitor to the MOSFET; and
  - an insulating structure encircling the contact, the insulating layer is capable of preventing the polysilicon layer from reacting with the contact structure.
47. The memory cell of claim 46, wherein the insulating structure is in contact with the polysilicon layer, the tungsten nitride layer, and the platinum-ruthenium layer.
48. The memory cell of claim 46, wherein platinum-ruthenium layer is separated from the polysilicon layer by the insulating structure.
49. A memory cell comprising:
  - a capacitor;
  - a transistor;
  - a contact structure coupling the capacitor to the transistor; and
  - an insulating structure encircling the contact structure.
50. The memory cell of claim 49, wherein the insulating structure is located between the contact and a borophosphosilicate glass layer.
51. The memory cell of claim 49, wherein the insulating structure is fabricated from tungsten nitride.
52. A memory cell comprising:
  - a capacitor;
  - a metal-oxide semiconductor field effect transistor (MOSFET);
  - a contact coupling the capacitor to the MOSFET; and

an oxide structure encircling the contact.

53. The memory cell of claim 52, wherein the oxide structure is in contact with a polysilicon layer.

54. The memory cell of claim 52, wherein an air gap separates the oxide structure from a polysilicon layer.

55. A memory cell comprising:

a capacitor;

a transistor;

a contact structure including a polysilicon layer, a tungsten nitride layer, and a ruthenium silicide layer, the contact structure coupling the capacitor to the transistor; and an insulating structure encircling the contact structure.

56. The memory cell of claim 55, wherein the transistor is a bipolar transistor.

57. The memory cell of claim 55, wherein the insulating layer is separated from the polysilicon layer by an air gap.

58. A memory cell comprising:

a capacitor;

a metal-oxide semiconductor field effect transistor (MOSFET);

a contact structure including a polysilicon layer, a tungsten nitride layer, and a platinum-ruthenium layer, the contact structure coupling the capacitor to the MOSFET; and

an insulating structure encircling the contact structure.

59. The memory cell of claim 58, wherein the insulating structure is in contact with the contact structure.

60. The memory cell of claim 58, wherein the insulating structure is in contact with the platinum-ruthenium layer.
61. A system comprising:  
a processor; and  
one or more memory cells coupled to the processor, wherein at least one of the memory cells includes a contact having an insulating structure capable of preventing a conductive layer from interacting with a barrier layer.
62. The system of claim 61, wherein the processor is a microprocessor.
63. The system of claim 61, wherein at least one of the memory cells is a dynamic random access memory (DRAM) cell.
64. A system comprising:  
a processor; and  
one or more dynamic random access memory (DRAM) cells coupled to the processor, wherein at least one of the DRAM cells includes a contact having an insulating structure capable of preventing interaction between a polysilicon layer and a barrier layer.
65. The system of claim 64, wherein the processor is a reduced instruction set (RISC) processor.
66. The system of claim 64, wherein the barrier layer prevents migration of oxygen atoms into a substrate.
67. A system comprising:  
a processor; and

- one or more dynamic random access memory (DRAM) cells coupled to the processor, wherein at least one of the DRAM cells includes a contact structure including a barrier structure fabricated from silicon nitride.
68. The system of claim 67, wherein the barrier structure encircles the contact structure.
69. The system of claim 67, wherein the contact structure includes one or more barrier layers.
70. A system comprising:  
a processor; and  
one or more memory cells, wherein at least one of the memory cells includes a contact structure having an insulating structure encircling the contact structure.
71. The system of claim 70, wherein the contact structure includes a polysilicon layer and two barrier layers.
72. The system of claim 70, wherein the contact structure includes a barrier layer capable of blocking migration of silicon atoms and a barrier layer capable of blocking migration of oxygen atoms.
73. A system comprising:  
a processor; and  
one or more dynamic random access memory (DRAM) cells coupled to the processor, wherein at least one of the DRAM cells includes a contact having a polysilicon layer, a tungsten nitride layer, and a ruthenium layer.
74. The system of claim 73, wherein the polysilicon layer is isolated from the ruthenium layer.

75. The system of claim 73, wherein the tungsten nitride layer is adjacent to the ruthenium layer.
76. A system comprising:
  - a processor; and
  - one or more dynamic random access memory (DRAM) cells coupled to the processor, wherein at least one of the DRAM cells includes a contact structure having a tungsten nitride layer, a ruthenium silicide layer, and an air gap encircling the tungsten nitride layer.
77. The system of claim 76, further comprising:
  - an oxide layer encircling the contact structure.
78. The system of claim 77, wherein the ruthenium silicide layer is in contact with the oxide layer.
79. A method comprising:
  - forming an active device on a substrate;
  - forming a passive device on the substrate; and
  - forming a contact structure including a barrier structure for coupling the passive device to the active device.
80. A method comprising:
  - forming a metal-oxide semiconductor field-effect transistor (MOSFET);
  - forming a passive device; and
  - forming a contact structure including a barrier structure capable of coupling the passive device to the MOSFET.
81. A method comprising:
  - forming a conductive layer on a base structure having a surface;

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- forming a first barrier layer above the conductive layer;  
etching the conductive layer and the first barrier layer to a level below the surface;  
forming a barrier structure that encircles the conductive layer and the first barrier  
layer;
- forming a second barrier layer above the first barrier layer; and  
polishing the second barrier layer and the surface.
82. The method of claim 81, further comprising:  
forming an active device below the conductive layer.
83. The method of claim 82, further comprising:  
forming a passive device above the second barrier layer.
84. A method comprising:  
forming a polysilicon layer on a base structure having a surface;  
forming a tungsten nitride layer above the conductive layer;  
etching the polysilicon layer and the tungsten nitride layer to a level below the  
surface;  
forming a silicon nitride structure that encircles the polysilicon layer and the  
tungsten nitride layer;  
forming a ruthenium silicide layer above the first barrier layer; and  
polishing the ruthenium silicide layer and the surface.
85. The method of claim 84, further comprising:  
forming a MOSFET below the conductive layer.
86. The method of claim 85, further comprising:  
forming a capacitor above the second barrier layer.

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87. A method comprising:  
forming a conductive layer on a base structure having a surface;  
forming a first barrier layer above the conductive layer;  
forming a second barrier layer above the first barrier layer;  
etching the first barrier layer and the second barrier layer;  
etching the conductive layer and the first barrier layer to a level below the surface;  
forming an oxide layer above the second barrier layer; and  
removing the oxide layer from above the second barrier layer.
88. The method of claim 87, further comprising:  
forming a transistor below the conductive layer.
89. The method of claim 88, further comprising:  
forming a passive device above the second barrier layer.
90. A method comprising:  
forming a polysilicon layer on a base structure having a surface;  
forming a tungsten nitride layer above the conductive layer;  
forming a ruthenium silicide layer above the tungsten nitride layer;  
etching the tungsten nitride layer and the ruthenium silicide layer;  
etching the polysilicon layer and the tungsten nitride layer to a level below the surface;  
forming an oxide layer above the ruthenium silicide layer; and  
removing the oxide layer from above the ruthenium silicide layer.
91. The method of claim 90, further comprising:  
forming an active device below the conductive layer.
92. The method of claim 91, further comprising:  
forming a capacitor above the second barrier layer.

93. A method of forming a contact, the method comprising:  
forming a structure having a plug volume above a substrate;  
forming a polysilicon layer in the plug volume;  
forming one or more barrier layers above the polysilicon layer;  
etching an outer perimeter to recess the outer perimeter of the plug volume down  
to a tungsten nitride layer;  
forming a barrier structure in the outer perimeter;  
etching the barrier structure to leave a sidewall above the tungsten nitride, but still  
expose the top surface;  
depositing the oxygen barrier layer to fill the rest of the plug; and  
polishing to isolate individual plug features.

